



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

[Handwritten signature]

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,778	06/27/2003	Mitsuo Usami	843.42897X00	6391
20457	7590	07/12/2005		EXAMINER
ANTONELLI, TERRY, STOUT & KRAUS, LLP 1300 NORTH SEVENTEENTH STREET SUITE 1800 ARLINGTON, VA 22209-3873			TUREMAN, JARED	
			ART UNIT	PAPER NUMBER
			2876	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,778	USAMI ET AL.	
	Examiner Jared J. Fureman	Art Unit 2876	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 28 April 2005.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-7 and 15-22 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-7 and 15-22 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 27 June 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>06/2003</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Receipt is acknowledged of the amendment, on 4/28/2005, which has been entered in the file. Claims 1-7 and 15-22 are pending.

Drawings

1. Figures 29-31 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated (see the background of the invention and the brief description of the drawings, in the specification). See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-7 and 17-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Derbenwick et al (US 6,900,536 B1).

Re claims 1, 3, 4, 15 and 16: Derbenwick et al teaches a semiconductor device (as shown in figure 5) comprising: an IC chip (integrated circuit 5, see figure 5 and column 5, lines 14-15) for wirelessly transmitting/receiving data; electrodes formed on a front surface (integrated circuit pad 30 serves as an electrode on a front surface of the IC 5, see figures 5, 6, and column 5, lines 18-20 and 39-47) and a rear surface of said IC chip (the back surface of IC 5 makes contact with substrate contact 33, see figures 5, 6 and column 5, lines 8-18, thus an electrode is necessarily present on the back surface of the IC 5); and a first conductor (conductive trace 32, see figure 5 and column 5, lines 6-7) and a second conductor (conductive trace 50, see figures 5, 6 and column 5, lines 15-18) connected (via substrate contacts 31 and 33) respectively to said electrodes, wherein said first conductor and said second conductor are connected outside said IC chip to form an antenna (the substrate contacts 31, 33 and conductive traces 32, 50 are all connected outside IC 5 to form an antenna, inductor coil 3, see figures 5, 6 and column 4, line 50 - column 5, line 67); a slit provided between said first conductor and said second conductor when viewed from a front surface side of said IC chip (the space between the first and second conductors, as shown in figure 5, may be considered a slit); a slit provided in said first conductor or said second conductor (the space between turns of the inductor coil 3, as shown in figure 5, may be considered a slit in the first or second conductor, since the space is a long and narrow opening); wherein said conductor in which said slit is provided is bent (conductive trace 32 is bent along fold line 35, see figure 5); wherein said conductor in which said slit is provided, before being

bent and connected to said electrode, is accommodated in the form of a rectangular shape (see figure 5).

Re claims 2 and 17-22: Derbenwick et al teaches a semiconductor device (as shown in figure 5) comprising: an IC chip (integrated circuit 5, see figure 5 and column 5, lines 14-15) for wirelessly transmitting/receiving data; a first electrode formed on a front surface of said IC chip (integrated circuit pad 30 serves as an electrode on a front surface of the IC 5, see figures 5, 6, and column 5, lines 18-20 and 39-47) and a second electrode formed on a rear surface of said IC chip (the back surface of IC 5 makes contact with substrate contact 33, see figures 5, 6 and column 5, lines 8-18, thus an electrode is necessarily present on the back surface of the IC 5); and a first conductor (conductive trace 32, see figure 5 and column 5, lines 6-7) and a second conductor (conductive trace 50, see figures 5, 6 and column 5, lines 15-18) connected (via substrate contacts 31 and 33) respectively to said first and second electrodes, wherein said second electrode, formed on the rear surface of said IC chip, has the same potential as that of a substrate (the back surface, for example) of said IC chip; wherein a slit provided between said first conductor and said second conductor when viewed from a front surface side of said IC chip (the space between the first and second conductors, as shown in figure 5, may be considered a slit); wherein a slit provided in said first conductor or said second conductor (the space between turns of the inductor coil 3, as shown in figure 5, may be considered a slit in the first or second conductor, since the space is a long and narrow opening); wherein at least one of said first or second conductors is bent (conductive trace 32 is bent along fold line 35, see figure 5); wherein

said conductor which is bent, before being bent and connected to said electrode, is accommodated in the form of a rectangular shape (see figure 5).

Re claims 5-7: Derbenwick et al teaches a wireless identification semiconductor device (as shown in figure 5) comprising: an IC chip (integrated circuit 5, see figure 5 and column 5, lines 14-15) for wirelessly transmitting/receiving data; electrodes formed on a front surface (integrated circuit pad 30 serves as an electrode on a front surface of the IC 5, see figures 5, 6, and column 5, lines 18-20 and 39-47) and a rear surface (the back surface of IC 5 makes contact with substrate contact 33, see figures 5, 6 and column 5, lines 8-18, thus an electrode is necessarily present on the back surface of the IC 5) of said IC chip; and a conductor having a slit and including a first portion and a second portion connected to said respective electrodes (inductor coil 3 includes a slit, the space between turns of the inductor coil 3 may be considered a slit, and includes a first portion, conductive trace 31 and substrate contact 31, and a second portion, conductive trace 50 and substrate contact 33, connected to said respective electrodes); wherein said conductor is bent (conductive trace 32 is bent along fold line 35, see figure 5) and connected to said electrodes; wherein said conductors before being bent and connected to said electrode is accommodated in the form of a rectangular shape (see figure 5).

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA

1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-6, 15, 17-19 and 21 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 7 (including the limitations of base claim 1) of copending Application No. 11/002,083 (hereinafter the '083 application). Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 7 of the '083 patent encompasses the scope of claims 1-6, 15, 17-19 and 21 of the present application. For example, claim 7 of the '083 application recites (including the limitations of base claim 1): An antenna connected to an IC chip that performs wireless identification, comprising a slit that separates two connection points with respect to the IC chip, wherein a length of the slit is approximately 3 millimeters, and a width of the slit is in a range of from 0.8 millimeter to 1.4 millimeters; wherein the antenna has an extending folded portion, the folded portion is folded to a position overlapping the antenna, the IC chip has terminals for connection on its both surfaces, and the antenna and the folded portion are connected to the IC chip.

Thus, while claim 7 of the '083 application uses different wording/terminology, it contains limitations corresponding to claims 1-6, 15, 17-19 and 21 of the present application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

6. The art made of record and not relied upon is considered pertinent to applicant's disclosure. Saito (US 6,795,025 B2), Yuichi (JP 2001-94031 A) and Sato et al (JP 2002-366917) all teach semiconductor devices including IC chips, electrodes and conductors having a bend and/or slit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared J. Fureman whose telephone number is (571) 272-2391. The examiner can normally be reached on 7:00 am - 4:30 PM M-T, and every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on (571) 272-2398. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

Art Unit: 2876

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jared J. Fureman
Jared J. Fureman
Primary Examiner
Art Unit 2876

July 7, 2005